IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Currently Amended): An ECC (Error Check and Correct) control apparatus to be connected between a host and a memory, comprising:

a data-path ~~first input/output~~ circuit which inputs and outputs data to and from the host, and inputs and outputs data to and from the memory;

a detecting circuit which detects a protected-data region and a redundant region of write data input ~~to the first input/output circuit~~ from the host and having a predetermined data length;

a code-generating circuit which generates an error-correction code for correcting errors in data of the protected-data region; and

a code-inserting circuit which inserts the error-correction code in the redundant region; ~~and~~

~~a second input/output circuit which inputs and outputs data to and from the memory~~

wherein the data-path circuit outputs the write data to the memory in synchronization with a first clock signal generated from a write-enable signal which is input from the host and indicates that data is being written into the memory.

Claim 2 (Original): The ECC control apparatus according to claim 1, which further comprises a counter which counts data items of the write data, and in which the detecting circuit detects the protected-data region and redundant region of the write data in accordance with a count value obtained by the counter.

Claim 3 (Original): The ECC control apparatus according to claim 2, wherein the detecting circuit detects a specified part of the redundant region, the code-generating circuit generates an error-correction code for correcting errors in the data of the protected-data region and the data of those parts of the redundant region which precede the specified part, and the code-inserting circuit inserts the error-correction code in the specified part of the redundant region.

Claim 4 (Currently Amended): The ECC control apparatus according to claim 3, further comprising a syndrome circuit which performs an syndrome operation on a read data input ~~to the second input/output circuit~~ from the memory and having the predetermined data length, by using the error-correction code contained in the read data, and which generates a syndrome signal, and an error-correcting circuit which corrects errors in accordance with the syndrome signal.

Claim 5 (Original): The ECC control apparatus according to claim 4, wherein the error-correcting circuit comprises an error-presence/absence determining circuit which determines whether the read data contains errors, and an error-information generating circuit which generates correction information for correcting errors, when the error-presence/absence determining circuit determines that the read data contains errors.

Claim 6 (Original): The ECC control apparatus according to claim 5, wherein the error-presence/absence determining circuit determines whether the number of erroneous data items has exceeded a predetermined value, when the error-presence/absence determining

circuit determines that the read data contains errors, and the error-information generating circuit generates abnormal-end information indicating that it is impossible to correct the read data, when the error-presence/absence determining circuit determines that the number of erroneous data items has exceeded the predetermined value.

Claim 7 (Original): The ECC control apparatus according to claim 5, wherein the error-information generating circuit generates normal-end information when the error-presence/absence determining circuit determines that the read data contains no errors.

Claim 8 (Currently Amended): The ECC control apparatus according to claim 2, in which the counter counts pulses that constitute ~~a write-enable signal inputting from the host and indicating that data is being written into the memory~~ the write-enable signal, and which further comprises ~~a clock-generating circuit which generates a first clock signal from the write-enable signal and~~ an enable interface circuit which does not output the write-enable signal to the memory when the number of pulses counted by the counter reaches a predetermined value.

Claim 9 (Currently Amended): The ECC control apparatus according to ~~claim 2~~ claim 20, in ~~wherein~~ which the counter counts pulses that constitute [[a]]the read-enable signal ~~inputting from the host and indicating that data is being read from the memory~~, and which further comprises ~~a clock-generating circuit which generates a second clock signal from the read-enable signal and~~ an enable interface circuit which does not output the read-enable signal to the memory when the number of pulses counted by the counter reaches a predetermined value.

Claim 10 (Currently Amended): The ECC control apparatus according to claim 8, wherein the counter starts counting the pulses after the ~~first input/output~~ data-path circuit receives an address signal that represents the address of the write data.

Claim 11 (Original): The ECC control apparatus according to claim 1, further comprising a register which registers a dummy chip-enable signal identical to a chip-enable signal indicating that the host is accessing the memory, and a chip-enable signal generating circuit which operates in a first mode to output to the memory the chip-enable signal received from the host and in a second mode to output the dummy chip-enable signal to the memory, thereby to supply the chip-enable signal or the dummy chip-enable signal to the memory by switching the first and second modes from one to the other.

Claim 12 (Original): The ECC control apparatus according to claim 6, in which the error-information generating circuit generates correction-end information when the error-presence/absence determining circuit determines that the number of erroneous data items has not exceeded the predetermined value, and which further comprises an interruption circuit which generates and supplies an interruption signal to the host to interrupt the host and an information output circuit which outputs the normal-end information or the abnormal-end information to the host when the interruption circuit supplies the interruption signal to the host.

Claim 13 (Original): The ECC control apparatus according to claim 1, which further comprises a region-changing circuit which changes that part of the redundant region which is

provided to store the error-correction code, and in which the code-inserting circuit inserts the error-correction code in that part of the redundant region which has been changed by the region-changing circuit.

Claim 14 (Original): The ECC control apparatus according to claim 1, further comprising a dedicated command circuit which performs a control not to output to the memory a command input from the host, once after a first command has been output from the host.

Claim 15 (Currently Amended): The ECC control apparatus according to claim 14, wherein the dedicated command circuit ~~comprises a circuit which~~ performs a control to output to the memory the command input from the host, ~~when~~ once after a second command is input from the host.

Claim 16 (Original): The ECC control apparatus according to claim 14, wherein the dedicated command circuit masks the write-enable signal input from the host, thereby not to write the command into the memory.

Claims 17-18 (Canceled).

Claim 19 (Original): The ECC control apparatus according to claim 1, wherein the memory is a NAND flash memory.

Claim 20 (New): The ECC control apparatus according to claim 4, wherein the data-path circuit outputs the read data to the host in synchronization with a second clock signal generated from a read-enable signal which is input from the host and indicates that data is being read from the memory.

Claim 21 (New): The ECC control apparatus according to claim 1, further comprising:

a plurality of delay-adjusting circuits which adjust delay times of control signals input from the host in accordance with wiring delays of the apparatus, the control signals including the write-enable signal; and

a clock circuit which generates the first clock signal from the write-enable signal adjusted by the delay-adjusting circuits.

Claim 22 (New): The ECC control apparatus according to claim 1, wherein the data-path circuit includes a latch circuit which latches the write data in accordance with the first clock signal.

Claim 23 (New): The ECC control apparatus according to claim 20, further comprising:

a plurality of delay-adjusting circuits which adjust delay times of control signals input from the host in accordance with wiring delays of the apparatus, the control signals including the read-enable signal; and

a clock circuit which generates the second clock signal from the read-enable signal adjusted by the delay-adjusting circuits.

Claim 24 (New): The ECC control apparatus according to claim 20, wherein the data-path circuit includes a latch circuit which latches the read data in accordance with the second clock signal.